REMARKS

Claims 1-7 are pending. In this Response, claim 3 is amended, and no new claims are added. Claims 1-7 are presented for examination.

Rejections Under 35 U.S.C. § 103

Claims 1, 4 and 7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Amini et al. (US 5,381,538, hereinafter Amini) in combination with Mills et al. (US 5,696,917, hereinafter Mills). The applicants respectfully traverse the rejection for at least the following reasons.

Claim 1 is directed to a programmable interface comprising, among other elements, "a register file having a plurality of registers, each register having a type," and "a run control register." The Action alleges that Amini discloses these elements. To purportedly show that Amini discloses "a register file having a plurality of registers," the Action points to Fig. 2 of Amini "wherein #104 is a 20 byte FIFO and #114 is a PIO register." Further, to purportedly show that Amini discloses "a run control register," the Action again points to Amini's PIO 114 in Fig. 2.[1] However, because of the different configurations of the recited "register file" and "run control register," Amini's PIO register cannot serve as both part of the "register file" and the "run control register." Therefore, Amini fails to teach at least one of the two elements.

Similarly, applicants respectfully submit that Amini does not disclose the recited feature "wherein the Code Store SRAM . . . [is] configured to bidirectionally communicate with a system processor." Claim 1 discloses "a Code Store SRAM configured to bidirectionally communicate with the microcontroller, . . . wherein the Code Store SRAM . . . [is] configured to bidirectionally communicate with a system processor." Thus, the Code Store SRAM is configured to bidirectionally communicate with a microcontroller and a system processor. An example of this configuration is shown in applicants' Fig. 1, where Code Store SRAM 14 is configured to bidirectionally communicate with microcontroller 12 and system processor 30. Applicants respectfully

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[1] The Action, page 3. Note that the Action actually states "[s]ee Figure 3 wherein #114 is a PIO register." However, applicant only finds a reference to PIO register 114 in Figure 2, and not Figure 3, so applicant

submit that Amini does not disclose this feature. The Action appears to equate Amini's microprocessor 30 from Fig. 1 with both the recited microcontroller and the recited system processor. However, the recited microcontroller and system processor are two distinct elements that are configured differently with respect to the other recited elements. Therefore, applicants respectfully submit that Amini at least does not disclose "a Code Store SRAM configured to bidirectionally communicate with the microcontroller, . . . wherein the Code Store SRAM . . . [is] configured to bidirectionally communicate with a system processor." Mills does not cure this deficiency of Amini.

Apart from the discussion above, the Action acknowledges that Amini does not disclose "executable code, loaded onto the Code Store SRAM; . . . wherein the system processor is configured to load the executable code onto the Code Store SRAM and is further configured to signal the microcontroller, via the run control register, to begin execution of one or more instructions included in the executable code." However, the Action alleges that Mills discloses these features.

Specifically, the Action cites a portion of Mills which states that "[i]n such a case, the program associated with the selected game will be loaded into SRAM 240 . . . . Moreover, the read/write files (including the executable code for the game) stored in battery backed SRAM 240 will not be lost." Mills, col. 10, lines 33-35, 50-52. While this arguably discloses executable code that is stored on SRAM, applicants respectfully submit that Mills does not disclose a "system processor configured to . . . signal the microcontroller, via the run control register, to begin execution of one or more instructions included in the executable code." (emphasis added). Although the Action seems to equate Mills' microprocessor 210 with the recited microcontroller, Mills does not disclose a "system processor" or a "run control register." Even if the executable code stored in SRAM allegedly taught by Mills is combined with the alleged system processor and run control register of Amini, the configuration of the system processor and run control register taught by Amini would not support a "system processor configured to . . . signal the microcontroller, via the run control register, to begin execution of one or more instructions included in the executable code." (emphasis

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will assume that the Action meant to reference Figure 2 in this instance.

added). Accordingly, applicants submit that neither Mills nor Amini, either alone or in combination, disclose this feature.

For at least the reasons stated above, applicants respectfully submit that claim 1 is allowable. Claims 4 and 7 depend from claim 1. Therefore, claims 4 and 7 are allowable for at least the reasons claim 1 is allowable.

Claims 2, 3, and 6 were rejected under 35 U.S.C. 103(a) as being unpatentable over Amini and Mills, in further view of Curry et al. (US 6,112,275, hereinafter Curry). Claims 2, 3, and 6 depend on independent claim 1. Curry teaches a method of communicating information between a host device and a potentially portable module device which measures thermal accumulation over time via a temperature controlled counter. Thus, it is respectfully submitted that Curry does not cure the deficiencies of Amini and Mills, as applied to claim 1. Therefore, claims 2, 3, and 6 are allowable for at least the reasons claim 1 is allowable.

Claim 5 was rejected under 35 U.S.C. 103(a) as being unpatentable over Amini and Mills, in further view of Ueda (US 5,631,637, hereinafter Ueda). Claim 5 depends from claim 1. Ueda teaches an output method for dot data enabling transmission and reception of data by cable or wireless. Thus, it is respectfully submitted that Ueda does not cure the deficiencies of Amini and Mills, as applied to claim 1. Therefore, claim 5 is allowable for at least the reasons claim 1 is allowable.

Conclusion

For at least these reasons, a Notice of Allowance is respectfully requested. If the Examiner has any questions concerning the present paper, the Examiner is kindly requested to contact the undersigned at (503) 796-2997. If any fees are due in connection with filing this paper, the Commissioner is authorized to charge Deposit Account No. 500393.

Respectfully submitted,
SCHWABE, WILLIAMSON & WYATT, P.C.

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/Kevin T. LeMond/
Kevin T. LeMond
Reg. No. 35,933

Pacwest Center, Suite 1600
1211 SW Fifth Avenue
Portland, Oregon 97204
Telephone: 503-222-9981